**ECEN 5863 - Programmable Logic Embedded System Design**

**Project Proposal**

**Project Title:** FPGA Audio Filter with Multi-Mode Switching using DE1 SoC FPGA

**Project Overview:**

This project aims to provide an interactive platform for users to explore and understand the diverse applications and effects of different audio filtering techniques in real-time using the DE1 SoC FPGA. By enabling users to experiment with various filter configurations using hardware switches. A user-friendly interface is introduced, allowing the user to dynamically toggle between five distinct audio filter options. The available choices include unfiltered audio for a direct pass-through, low pass filter, high pass filter, band pass filter and All-pass filter.

The project focuses on building an FPGA-based audio processing system that integrates essential modules such as a clock generator, Audio CODEC Interface, and Audio/Video Configuration. This foundational setup as in the Project 3 Module 2 facilitates audio recording from a microphone and playback through speakers.

**Implementation Stages:**  
**Stage 1:** Implementing each filter individually involves meticulously developing and testing the Unfiltered, Low-Pass, High-Pass, Band-Pass, and All-Pass filters within the existing Project 3Module2 setup. This stage focuses on refining filter algorithms for optimal performance and conducting thorough testing to ensure accuracy.

**Stage 2:** During the integration phase, five switches are designated for dynamic user control:

* **Switch 1 (Unfiltered):** Enables the direct pass-through of the original audio signal without any filtering.
* **Switch 2 (Low-Pass):** Activates the digital low-pass filter, allowing frequencies below a set cutoff to pass through while attenuating higher frequencies.
* **Switch 3 (High-Pass):** Triggers the digital high-pass filter, permitting frequencies above a designated cutoff to pass through while attenuating lower frequencies.
* **Switch 4 (Band-Pass):** Engages the digital Band-Pass Filter, facilitating the passage of a specific frequency range, showcasing the system's versatility.
* **Switch 5 (All-Pass):** This filter serves as a straightforward pathway, showcasing how the audio signal seamlessly passes through the entire array of available filters in the system

**Stage3:**

Integrating the HPS (Hard Processor System) into the FPGA enhances user control over the audio filtering system. The HPS is utilized for dynamic management and switching between filtering options, providing a more sophisticated user interface.

**A computer screen shot of a computer

Description automatically generated**

**Block Diagram**